Multi-Pattern Active Cell Balancing Architecture and Equalization Strategy for Battery Packs

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ABSTRACT

Active cell balancing is the process of improving the usable capacity of a series-connected Lithium-Ion (Li-Ion) battery pack by redistributing the charge levels of individual cells. Depending upon the State-of-Charge (SoC) distribution of the individual cells in the pack, an appropriate charge transfer pattern (cell-to-cell, cell-to-module, module-to-cell or module-to-module) has to be selected for improving the usable energy of the battery pack. However, existing active cell balancing circuits are only capable of performing limited number of charge transfer patterns and, therefore, have a reduced energy efficiency for different types of SoC distribution. In this paper, we propose a modular, multi-pattern active cell balancing architecture that is capable of performing multiple types of charge transfer patterns (cell-to-cell, cell-to-module, module-to-cell and module-to-module) with a reduced number of hardware components and control signals compared to existing solutions. We derive a closed-form, analytical model of our proposed balancing architecture with which we profile the efficiency of the individual charge transfer patterns enabled by our architecture. Using the profiling analysis, we propose a hybrid charge equalization strategy that automatically selects the most energy-efficient charge transfer pattern depending upon the SoC distribution of the battery pack and the characteristics of our proposed balancing architecture. Case studies show that our proposed balancing architecture and hybrid charge equalization strategy provide up to a maximum of 46.83% improvement in energy efficiency compared to existing solutions.

CCS Concepts

•**Hardware** → **Batteries;** •**Computing methodologies** → *Modeling methodologies;* •**Computer systems organization** → *Embedded hardware;*

Keywords

Batteries, active cell balancing, equalization algorithms

1 Introduction

Battery packs for high power applications such as Electric Vehicles (EVs) are formed of multiple Lithium-Ion (Li-Ion) cells that are connected in series to satisfy the high operating voltage required for the application. Manufacturing differences and varying temperature distribution along the battery pack lead to variation in the State-of-Charge (SoC) of individual cells in the battery pack.

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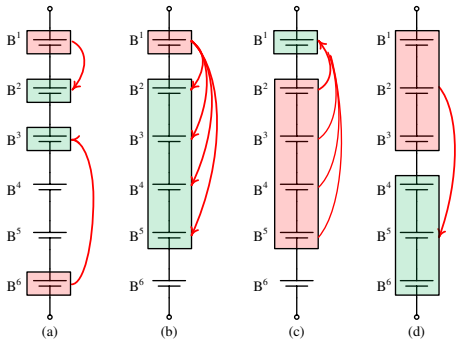


Figure 1: (a) Cell-to-Cell, (b) Cell-to-Module, (c) Module-to-Cell and (d) Module-to-Module.

This reduces the usable capacity of the battery pack since a series-connected pack can only be discharged till any cell in the pack reaches its lower SoC threshold. Subsequently, the charging process is also affected by the charge variations since any cell reaching the top threshold will stop the charging process. This leads to an unusable battery pack where the cell with high SoC compared to others limits the charging process and the cell with the least SoC determines the discharging threshold.

Cell balancing is typically performed to equalize the SoC of all cells in the pack [2]. *Passive* balancing approaches, see [9], are energy-inefficient, since the excess charge in each cell is dissipated as heat across a high power resistor that is attached with each cell. By contrast, *active* cell balancing approaches, see [4], increase the usable capacity of the battery pack by redistributing the excess charge between cells, instead of dissipating it.

Problem motivation: Based on the type of charge transfer pattern, active cell balancing architectures are classified into cell-to-cell, cell-to-module, module-to-cell and module-to-module as shown in Fig. 1, where a module is defined as a collection of cells (B^2, B^3, B^4 and B^5 in Fig. 1b). As we will show in Section 5, selecting an appropriate charge transfer pattern depending upon the SoC distribution of the battery pack, vastly increases the usable capacity of the battery pack. However, the circuit configuration of existing active cell balancing architectures limits their flexibility in performing multiple types of charge transfer patterns. For instance, the balancing architectures proposed in [11] and [5] are only capable of performing cell-to-cell charge transfers, since their circuit configuration allows only a single cell to be connected as input and output to the balancing architecture. Similarly, the architecture in [1] has its input and output fixed to a module and a single cell, respectively, thereby enabling only transfers between cell-to-module and vice versa. In order to enable multiple charge transfer patterns, either more switches are required or a complex control scheme with multiple high frequency control signals must be used, where in both cases the energy efficiency is also reduced. Therefore, active cell balancing architectures that can support multiple types of charge transfer patterns with a reduced number of switches and a simpler control scheme will have improved performance as we will show in Section 6. In addition to the architectural flexibility, a smart equalization strategy that selects the energy-efficient charge transfer pattern depending upon the SoC distribution and the characteristics of the underlying balancing circuit is required to fully utilize the potentials of the given balancing architecture.

Contributions and organization: The major contributions of this paper are:

1. We propose a modular, multi-pattern active cell balancing architecture in Section 3, that can perform multiple charge transfer patterns shown in Fig. 1, with a reduced number of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and a simple control scheme in comparison to the state-of-the-art. We use a charge transfer bus for interfacing the cells that need to send or receive charge for facilitating the different types of charge transfer patterns.
2. In Section 4, we derive a closed-form analytical model of our proposed balancing architecture and using this analytical model, in Section 5, we compare the energy efficiency of the individual charge transfer patterns for different types of realistic SoC distributions. With this profiling analysis, we propose a hybrid charge transfer strategy in Section 5 that dynamically selects the energy-efficient charge transfer pattern depending upon the SoC distribution of the cells in the pack.
3. Case studies performed in Section 6 show that, our proposed modular balancing architecture and the hybrid charge transfer strategy provide up to 46.83 % improvement in energy efficiency compared to state-of-the-art solutions.

Finally, Section 7 gives concluding remarks.

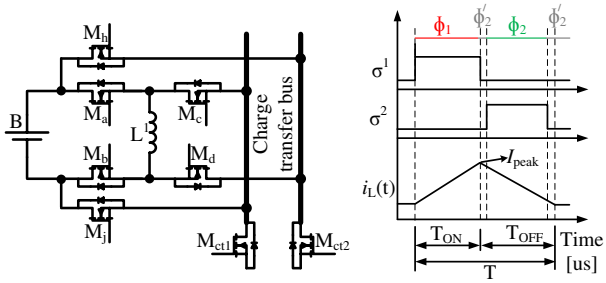
2 Related Work

Balancing architectures: Existing active cell balancing architectures are typically limited regarding the number of charge transfer patterns they can perform. For instance, the architecture in [12] is capable of performing cell-to-cell charge transfer only between adjacent cells in the pack. However, the temperature gradient in a battery pack results in an imbalance in SoC of cells that are not adjacent in the series string of the pack. Even though, the direct non-neighbor charge transfer architectures proposed in [7] and [5] require additional switches, they provide higher efficiency compared to the neighbor-only balancing architectures as shown in [5]. Therefore, we are mainly interested in architectures that are capable of performing direct charge transfers between non-adjacent cells in the pack. However, [7] and [5] are capable of only performing a cell-to-cell charge transfer pattern and are not flexible to enable multiple balancing patterns. By contrast, our proposed architecture supports direct non-neighbor balancing and, in addition, enables multiple charge transfer patterns shown in Fig. 1, with fewer MOSFETs compared to [5] (10 MOSFETs are used in [5] while we have only 8 switches) and less control signals compared to [7] ([7] requires 3 high frequency control signals while we need only 2). While the many-to-many balancing architecture proposed in [6] supports multiple charge transfer patterns, it does not enable direct non-neighbor balancing and also has a higher resistance over the charge transfer path compared to our proposed architecture. Since the efficiency of the equalization process is significantly influenced by the resistance along the charge transfer path, our proposed balancing architecture, by having a reduced charge transfer resistance, dominates the existing approaches in terms of energy efficiency for different types of SoC distribution as will be shown in Section 6.

Balancing strategies: Balancing strategies determine the source and destination cells of the charge transfer pair considering the SoC distribution of the battery pack and the capabilities of the underlying balancing architecture. For instance, in [3], strategies for maximizing the capacity and energy of a battery pack using a neighbor-only, capacitor-based architecture were proposed. Similarly, heuristics for equalizing the SoC of cells in a battery pack using an inductor-based, non-neighbor and neighbor-only balancing architectures were proposed in [5] and [10], respectively. However, these strategies are designed for balancing architectures that do not support multiple charge transfer patterns and, therefore, cannot fully exploit the flexibility of our proposed architecture. Here, a new balancing strategy is required to fully utilize the potentials of the different charge transfer patterns enabled by our proposed architecture. We profile the efficiencies of the different charge transfer patterns enabled by our architecture and we propose a hybrid charge equalization algorithm in Section 5 that selects the energy-efficient transfer pattern considering the resistances along the current flow path and the SoC distribution.

3 Proposed Modular Balancing Architecture

In this section, we describe the homogeneous module of our proposed balancing architecture and its capability to perform the different types of charge transfer patterns shown in Fig. 1.



(a) Modular balancing unit

(b) Control signals and the balancing current

Figure 2: (a) Homogeneous unit of our proposed modular balancing architecture consisting of 8 power MOSFET switches and one inductor. (b) High frequency control signals and the corresponding balancing current through the inductor.

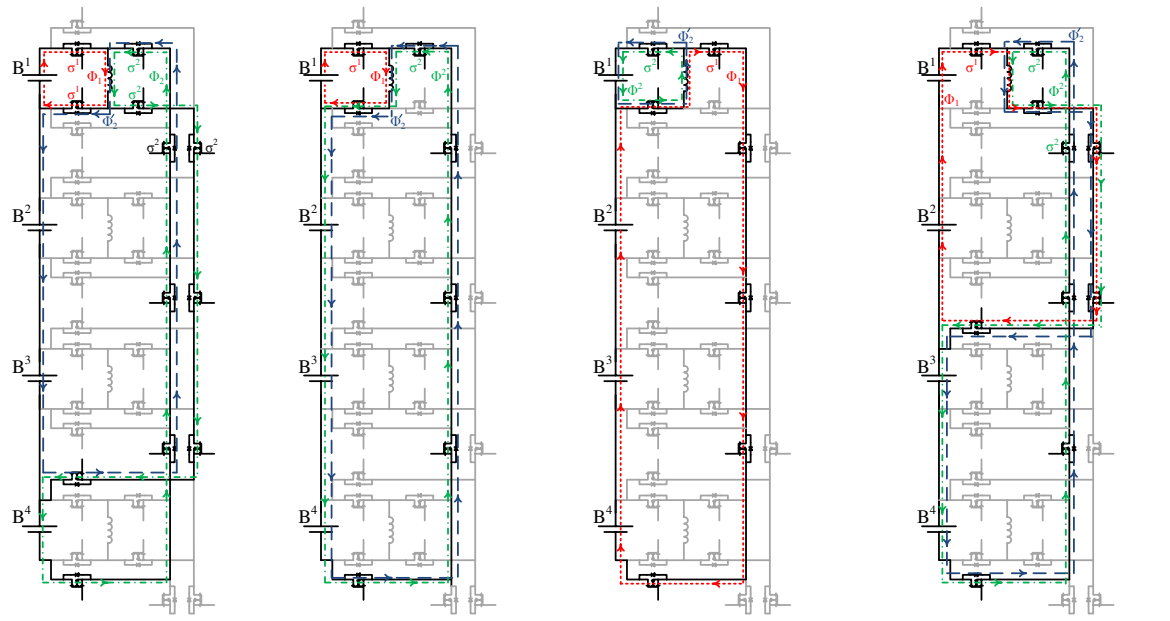
3.1 Modular Balancing Unit

Fig. 2a shows an individual module of our proposed balancing architecture attached to each cell of the battery pack. Note that the battery cell might be a single high energy cell or a parallel connection of multiple low energy cells and only a single balancing unit is required for each group of parallel-connected cells. Moreover, the balancing module is attached as an external unit to the cell without interrupting the main powerline of the pack and therefore enabling equalization while that pack is in operation (both charging and discharging). Each balancing module consists of one inductor (L^1) and eight power MOSFET switches as shown in Fig. 2a. The energy storage element (inductor) is connected to the respective battery cell and the charge transfer bus through switches M_a, M_b and M_c, M_d, respectively. MOSFETs M_h and M_j connect the battery cell directly to the charge transfer bus. M_{ct1} and M_{ct2} are used to isolate the charge transfer bus for enabling different types of charge transfer patterns as will be shown in Section 3.2. Balancing is enabled by actuating a certain set of MOSFET switches with non-overlapping high frequency control signals (σ^1 and σ^2) as shown in Fig. 2b and a certain set of switches with static *ON* or *OFF* control signals, as explained in the working principle in the next section.

3.2 Charge Transfer Patterns

Here, we explain the operating principle and show the different charge transfer patterns enabled by our proposed architecture.

Working principle: For the following explanation, please refer to Fig. 3a, where a direct non-neighbor charge transfer between cell B^1 and B^4 is shown. First, the switches that are statically controlled with *ON* or *OFF* signals are actuated to establish the path for balancing current. In this example, switches M_h^4 and M_j^4 are turned *ON* to connect the destination cell (B^4) to the charge transfer bus and the source cell (B^1) is isolated from the charge transfer bus by turning *OFF* the switches M_h^1 and M_j^1, respectively. Charge transfer bus MOSFETs (M_{ct1}^2, M_{ct2}^2, M_{ct1}^3 and M_{ct2}^3) in the modules that are in between the source and destination cells are turned *ON* in order to provide the balancing current flow path to the destination cell B^4. After initializing all the switches that are statically turned *ON* or *OFF*, the charge transfer between the cells takes place by actuating the switches in the source cell module with non-overlapping high frequency control signals. Here switches M_a^1 and M_b^1 are first actuated with the control signal σ^1 shown in Fig. 2b. The current through the inductor rises linearly till I_{peak} (marked as phase Φ_1 in Fig. 2b), storing the excess energy from source cell B^1. Once the MOSFETs M_a^1 and M_b^1 are turned *OFF*, the current through the inductor freewheels through cells B^2 and B^3 as marked as phase Φ_2' in Fig. 3a. This freewheeling is necessary to avoid any short circuit conditions between cells since there exist a certain delay for the MOSFETs to change their state from *ON* to *OFF* or vice versa. The stored energy in the inductor is transferred to the destination cell (B^4) during the discharging phase (marked



Top-to-Bottom	
R_α	$R_{B^\alpha} + R_L + 2 \cdot R_M$
R_β	$R_{B^\beta} + R_L + (6 + 2 \cdot d) R_M$
Bottom-to-Top	
R_α	$R_{B^\alpha} + R_L + (6 + 2 \cdot d) R_M$
R_β	$R_{B^\beta} + R_L + 2 \cdot R_M$

(a) Cell-to-Cell

Top-to-Bottom	
R_α	$R_{B^\alpha} + R_L + 2 \cdot R_M$
R_β	$n^\delta \cdot R_{B^\beta} + R_L + (3 + n^\delta) R_M$
Bottom-to-Top	
R_α	$R_{B^\alpha} + R_L + (4 + 2 \cdot n^\delta) R_M$
R_β	$n^\delta \cdot R_{B^\beta} + R_L + (3 + n^\delta) R_M$

(b) Cell-to-Module

Top-to-Bottom	
R_α	$n^\sigma \cdot R_{B^\alpha} + R_L + (3 + n^\sigma) R_M$
R_β	$R_{B^\beta} + R_L + (3 + 2 \cdot n^\sigma) R_M$
Bottom-to-Top	
R_α	$n^\sigma \cdot R_{B^\alpha} + R_L + (3 + n^\sigma) R_M$
R_β	$R_{B^\beta} + R_L + 2 \cdot R_M$

(c) Module-to-Cell

Top-to-Bottom	
R_α	$n^\sigma \cdot R_{B^\alpha} + R_L + (3 + n^\sigma) R_M$
R_β	$n^\delta \cdot R_{B^\beta} + R_L + (3 + 2 \cdot n^\sigma + n^\delta) R_M$
Bottom-to-Top	
R_α	$n^\delta \cdot R_{B^\alpha} + R_L + (3 + n^\sigma + 2 \cdot n^\delta) R_M$
R_β	$n^\delta \cdot R_{B^\beta} + R_L + (3 + n^\delta) R_M$

(d) Module-to-Module

Figure 3: Multiple charge transfer patterns enabled by our proposed architecture (a) Cell-to-Cell ($B^1 \rightarrow B^4$). (b) Cell-to-Module ($B^1 \rightarrow B^2, B^3, B^4$). (c) Module-to-Cell ($B^2, B^3, B^4 \rightarrow B^1$). (d) Module-to-Module ($B^1, B^2 \rightarrow B^3, B^4$).

as Φ_2 in Fig. 2b) by actuating the MOSFETs M_c^1, M_d^1, M_{ct1}^1 and M_{ct2}^1 with the complementary control signal σ^2. Finally, a single charge transfer cycle is completed by transferring the last remaining energy through the freewheeling path Φ_2', ensuring that the inductor is not charged in the opposite direction.

Balancing patterns: Fig. 3 shows the capability of our proposed balancing architecture to perform multiple charge transfer schemes. All charge transfer patterns are verified for functionality and possible short circuits using a SPICE simulation. In Fig. 3b, a cell-to-module charge transfer pattern is shown where excess charge from cell B^1 is transferred to cells B^2, B^3 and B^4. This type of transfer will be beneficial in case of *top balancing*, where a single cell with high SoC is resulting in a premature cut-off of the charging process and quickly redistributing its excess charge to other cells will minimize the overall charging time. Similarly, the module-to-cell transfer pattern as shown in Fig. 3c, is advantageous in case of *bottom balancing*, where the excess charge in cells B^2, B^3 and B^4 is quickly redistributed to a single weak cell B^1, thereby preventing premature cut-off of the discharging process. Finally, the module-to-module transfer scheme shown in Fig. 3d enables equalization between modules, where a single module consists of a certain number of cells that have the same charge level.

4 Analytical Model

In this section, we derive an analytical model of our proposed balancing architecture that will be used for our case study in Section 6.

4.1 Balancing Current and Charge Model

We use an electrical equivalent circuit model of Li-Ion cells that has been extensively researched in the literature and validated, for instance, in [8]. The electrical cell model consists of a voltage source in series with the internal resistance of the cell and two *RC*-networks modeling the transient response as shown in Fig. 4. Fig. 4a and 4b show the equivalent circuits of the balancing architecture during phases Φ_1 and Φ_2 of the charge transfer process, respectively. Our model ignores the short freewheeling phases Φ_2' due to their relatively small values (in the range of ns) compared to the phases Φ_1 and Φ_2 which occur in the range of µs.

Equivalent Phase Φ_1: By applying KIRCHHOFF's mesh rule to Fig. 4a results in the following equation

$$V_{B^\alpha} - V_{B^\alpha}^{ts} - V_{B^\alpha}^{tl} = L \cdot \frac{d}{dt} i_\alpha(t) + R_\alpha \cdot i_\alpha(t) \tag{1}$$

where V_{B^α} is the open circuit voltage across the source cell B^α, $V_{B^\alpha}^{ts}$ and $V_{B^\alpha}^{tl}$ are the voltages across the two *RC*-networks, respectively. R_α is the sum of the parasitic resistances of the circuit components in the current flow path. Combining V_{B^α}, $V_{B^\alpha}^{ts}$ and $V_{B^\alpha}^{tl}$ into a single term V_{C^α} and solving Eq. (1) with the initial value of the inductor current as $i(0) = 0$ gives:

$$i_\alpha(t) = \frac{V_{C^\alpha}}{R_\alpha} \left(1 - e^{-\frac{R_\alpha}{L} t}\right) \tag{2}$$

The time T_{ON} required for the inductor current to reach I_{peak} and the charge Q_{tx} taken out of the source cell are given by:

$$T_{ON} = \frac{L}{R_\alpha} \cdot \ln \left[\frac{V_{C^\alpha}}{V_{C^\alpha} - R_\alpha \cdot I_{peak}}\right] \tag{3}$$

$$Q_{tx} = \frac{V_{C^\alpha}}{R_\alpha} T_{ON} + \frac{L \cdot V_{C^\alpha}}{R_\alpha^2} \left(e^{\frac{-R_\alpha}{L} T_{ON}} - 1\right) \tag{4}$$

Equivalent Phase Φ_2: Similar deductions for the equivalent circuit shown in Fig. 4b using KIRCHHOFF's mesh rule and solving for the inductor discharge current $i_\beta(t)$ yields

$$i_\beta(t) = I_{peak} \left(e^{-\frac{R_\beta}{L} t}\right) - \frac{V_{C^\beta}}{R_\beta} \left(1 - e^{-\frac{R_\beta}{L} t}\right) \tag{5}$$

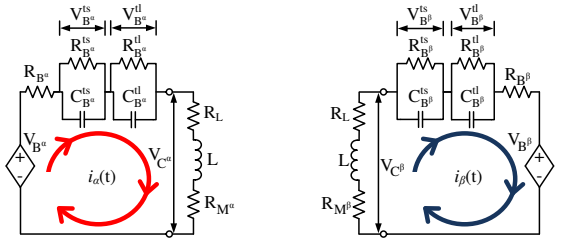


Figure 4: Equivalent circuits for each phase of the charge transfer process. (a) The inductor is charged during phase Φ_1 by the source cell and (b) discharged to the destination cell during the phase Φ_2.

where $V_{C\beta}$ is the sum of the voltage drops across the *RC*-networks in the destination cell and the open circuit voltage of the cell and R_β is the equivalent parasitic resistance of the circuit components. The initial value of the discharging current $i_\beta(t)$ is the peak value of the balancing current $i_\beta(0) = I_{\text{peak}}$ during the charging phase. The time taken to discharge the inductor current and the charge Q_{rx} that is received by the destination cell is then obtained by:

$$T_{\text{OFF}} = \frac{L}{R_\beta} \cdot \ln\left(\frac{V_{C\beta} + R_\beta \cdot I_{\text{peak}}}{V_{C\beta}}\right) \tag{6}$$

$$Q_{\text{rx}} = \frac{L}{R_\beta}\left(I_{\text{peak}} + \frac{V_{C\beta}}{R_\beta}\right)\left[1 - e^{-\frac{R_\beta}{L}T_{\text{OFF}}}\right] - \frac{V_{C\beta}}{R_\beta}T_{\text{OFF}} \tag{7}$$

4.2 Energy Efficiency

The energy efficiency of the balancing process is defined as the ratio of energy dissipated to the energy transferred.

$$\eta_{\text{eff}} = 1 - \frac{E_{\text{diss}}}{E_{\text{tx}}} \tag{8}$$

Energy dissipation (E_{diss}): The parasitic resistances present in the circuit components dissipate heat when a current flows through them, referred to as conduction energy dissipation obtained by:

$$\begin{aligned} E^{\text{cd}}_{\text{cyc}} &= E_{\text{tx}} - E_{\text{rx}} \\ &= Q_{\text{tx}} \cdot V_{C\alpha} - Q_{\text{rx}} \cdot V_{C\beta} \end{aligned} \tag{9}$$

Moreover, each switching activity of the MOSFET involves charging and discharging of input and output parasitic capacitances resulting in non-zero turn-on (t_{ON}) and turn-off (t_{OFF}) delays.

$$E^{\text{sw}}_{\text{cyc}} = \frac{1}{2}I_{\text{peak}}\left(t_{\text{OFF}} \cdot V_{C\alpha} + t_{\text{ON}} \cdot V_{C\beta}\right) + \frac{1}{2}C_{\text{OSS}}\left(V^2_{C\alpha} + V^2_{C\beta}\right) \tag{10}$$

The total energy dissipation (E_{diss}) is obtained by:

$$E_{\text{diss}} = E^{\text{cd}}_{\text{cyc}} + E^{\text{sw}}_{\text{cyc}} \tag{11}$$

5 Hybrid Charge Transfer Strategy

In this section, we explain our hybrid charge equalization strategy that automatically selects the energy-efficient charge transfer pattern depending upon the SoC distribution and the characteristics of our balancing architecture.

5.1 Profiling Analysis

Even though multiple charge transfer patterns are enabled by our architecture, depending upon the SoC distribution pattern and the characteristics of the underlying hardware circuit, an appropriate strategy must be selected for improving the efficiency of the balancing process. We profile the efficiencies of the individual charge transfer patterns for different types of realistic SoC distributions. For this purpose, we first explain the methodology for determining the balancing pair for different types of charge transfer patterns enabled by our architecture. We assume that there exists a Battery Management System (BMS) that can calculate the SoC of all the cells in the pack and the following algorithms use this information

Algorithm 1 Cell-to-Module charge transfer algorithm.

Input: Unbalanced SoC array $\mathcal{U}$, Maximum transfer length M
Output: Charge transfer pairs $\mathcal{P}$

1: $\overline{\mathcal{U}}$ =mean($\mathcal{U}$), $\mathcal{B} = \{1, 2, ...N\}$, $\mathcal{P} = \{\}$
2: **while** $\mathcal{B} \neq \{\}$ **do**
3: $s = \text{argmax}(\mathcal{U})$
4: **if** $s = 1$ or $\overline{\mathcal{U}_{s-M}} > \overline{\mathcal{U}_{s+M}}$ **then**
5: $di = 1$
6: **else if** $s = N$ or $\overline{\mathcal{U}_{s-M}} < \overline{\mathcal{U}_{s+M}}$ **then**
7: $di = -1$
8: **end if**
9: $S = \{s\}$, $D = \{\}$
10: **while** $\mathcal{U}_{s+di} < \overline{\mathcal{U}}$ and $|di| < M$ **do**
11: $D = D \cup \{s + di\}$
12: **if** $di > 0$ **then**
13: $di = di + 1$ (Expand to the right)
14: **else**
15: $di = di - 1$ (Expand to the left)
16: **end if**
17: **end while**
18: $\mathcal{P} = \mathcal{P} \cup \{(S, D)\}$
19: **if** $D \neq \{\}$ **then**
20: $\mathcal{B} = \mathcal{B} \backslash \{min(S \cup D), min(S \cup D) + 1, ..., max(S \cup D)\}$
21: **else**
22: $\mathcal{B} = \mathcal{B} \backslash \{s\}$
23: **end if**
24: **end while**

to identify the charge transfer pairs.

Cell-to-Module (C2M): Algorithm 1 shows the methodology for determining the source cell and the destination module for a cell-to-module charge transfer pattern explained in Fig. 3b. The input to the algorithm is the SoC distribution ($\mathcal{U}$) and the maximum number of cells that could be included in the destination module defined by M. The value of M is limited by the drain-to-source voltage of the MOSFETs in the balancing architecture, which has to block the sum of the nominal voltages of the cells in the destination module. The output of the algorithm will provide the charge transfer pairs $\mathcal{P}$ consisting of the index of the source cell and the destination module. Initially, the set $\mathcal{P}$ is empty and the index of the cells is stored in the set $\mathcal{B}$ (line 1). As the algorithm finds the transfer pairs, they are added to set $\mathcal{P}$ and subsequently removed from $\mathcal{B}$. The algorithm executes till the index set $\mathcal{B}$ is empty (line 2). As explained in Section 3.2, the general idea of doing a cell-to-module charge transfer is to rapidly redistribute the excess charge stored in a single cell to the remaining cells in the pack. Therefore, we start with finding the source cell which is the cell with the highest SoC compared to other cells in the pack (line 3). The direction of transfer di is determined by the position of the source cell and the overall average charge ($\overline{\mathcal{U}_{s-M}}$ and $\overline{\mathcal{U}_{s+M}}$) on both sides of the source cell (lines 4 - 8). After identifying the charge transfer direction di, the cells in that direction are included in the destination list D if their SoC is below the global average value ($\overline{\mathcal{U}}$) and they are within the maximum range defined by M (lines 10 - 17). Subsequently, the charge transfer pair list $\mathcal{P}$ is updated and the corresponding cells are removed from the index set $\mathcal{B}$ (lines 18 - 23).

Module-to-Cell (M2C): For the following explanation, please refer to Algorithm 2. The motivation for module-to-cell transfer pattern is to quickly charge the weak cell in the pack in order to prevent premature cut-off of the discharging process. Therefore, the module-to-cell transfer algorithm first starts with identifying the destination cell that is the cell with the least SoC among all cells in the pack (line 3). Moreover, the direction from which side to receive charge is determined by comparing the average value of SoC on both sides (lines 4 - 8). The source cell list S is updated with the index of cells in the charge transfer direction if their SoC is greater than the global average and the number of cells in the source list is within M (lines 10 - 17).

Module-to-Module (M2M): The module-to-module transfer algorithm described in Algorithm 3 starts with first identifying the source module that has cells with SoC above the average SoC of the pack (lines 3 - 14). The mean on both sides of the source module is checked to identify the direction of charge transfer and the cells in the destination set (lines 15 - 25). The pair list $\mathcal{P}$ is updated with the source and destination cell sets (line 26) and the corre-

Algorithm 2 Module-to-Cell charge transfer algorithm.

Input: Unbalanced SoC array $\mathcal{U}$, Maximum transfer length M
Output: Charge transfer pairs $\mathcal{P}$

$\overline{\mathcal{U}}$ =mean($\mathcal{U}$), $\mathcal{B} = \{1, 2, ...N\}$, $\mathcal{P} = \{\}$
while $\mathcal{B} \neq \{\}$ **do**
  $d = \text{argmin}(\mathcal{U})$
  if $d = 1$ or $\overline{\mathcal{U}_{d-M}} < \overline{\mathcal{U}_{d+M}}$ **then**
    $di = 1$
  else if $d = N$ or $\overline{\mathcal{U}_{d-M}} > \overline{\mathcal{U}_{d+M}}$ **then**
    $di = -1$
  end if
  $D = \{d\}$, $S = \{\}$
  while $\mathcal{U}_{d+di} > \overline{\mathcal{U}}$ and $|di| < M$ **do**
    $S = S \cup \{d + di\}$
    if $di > 0$ **then**
      $di = di + 1$ (Expand to the right)
    else
      $di = di - 1$ (Expand to the left)
    end if
  end while
  $\mathcal{P} = \mathcal{P} \cup \{(S, D)\}$
  if $S \neq \{\}$ **then**
    $\mathcal{B} = \mathcal{B} \backslash \{min(S \cup D), min(S \cup D) + 1, ..., max(S \cup D)\}$
  else
    $\mathcal{B} = \mathcal{B} \backslash \{d\}$
  end if
end while

sponding cells are removed from $\mathcal{B}$ for next iteration (lines 27 - 31).

Cell-to-Cell (C2C): Please note that the cell-to-cell transfer pattern has been extensively studied in the literature and in this paper we adopt the *fast* strategy that is proposed in [5]. Here, the source cell with the highest SoC is paired with the destination cell, which is the cell with the lowest SoC within the module range M. The cells in between the charge transfer pairs remain blocked and the algorithm repeats till no pairs can be included in the pair list ($\mathcal{B} = \{\}$).

Profiling setup: We performed several balancing simulations with

Algorithm 3 Module-to-Module charge transfer algorithm.

Input: Unbalanced SoC array $\mathcal{U}$, Maximum transfer length M
Output: Charge transfer pairs $\mathcal{P}$

$\overline{\mathcal{U}}$ =mean($\mathcal{U}$), $\mathcal{B} = \{1, 2, ...N\}$, $\mathcal{P} = \{\}$
while $\mathcal{B} \neq \{\}$ **do**
  $s = \text{argmax}(\mathcal{U})$, $m_r = m_l = m_d = 1$, $S = \{\}$, $D = \{\}$
  while $m_r + m_l \leq \lfloor \frac{M}{2} \rfloor$ **do**
    if $\mathcal{U}_{s+m_r} > \overline{\mathcal{U}}$ **then**
      $S = S \cup \{s + m_r\}$
      $m_r = m_r + 1$
    else if $\mathcal{U}_{s-m_l} > \overline{\mathcal{U}}$ **then**
      $S = S \cup \{s - m_l\}$
      $m_l = m_l + 1$
    else
      break
    end if
  end while
  if $S \neq \emptyset$ and $\overline{\mathcal{U}_{\text{min}(S)-\lfloor \frac{M}{2} \rfloor}} > \overline{\mathcal{U}_{\text{max}(S)+\lfloor \frac{M}{2} \rfloor}}$ **then**
    while $\mathcal{U}_{max(S)+m_d} < \overline{\mathcal{U}}$ and $m_d < \lfloor \frac{M}{2} \rfloor$ **do**
      $D = D \cup \{max(S) + m_d\}$
      $m_d = m_d + 1$
    end while
  else if $S \neq \emptyset$ and $\overline{\mathcal{U}_{\text{min}(S)-\lfloor \frac{M}{2} \rfloor}} < \overline{\mathcal{U}_{\text{max}(S)+\lfloor \frac{M}{2} \rfloor}}$ **then**
    while $\mathcal{U}_{min(S)-m_d} < \overline{\mathcal{U}}$ and $m_d < \lfloor \frac{M}{2} \rfloor$ **do**
      $D = D \cup \{min(S) - m_d\}$
      $m_d = m_d + 1$
    end while
  end if
  $\mathcal{P} = \mathcal{P} \cup \{(S, D)\}$
  if $D \neq \{\}$ **then**
    $\mathcal{B} = \mathcal{B} \backslash \{min(S \cup D), min(S \cup D) + 1, ..., max(S \cup D)\}$
  else
    $\mathcal{B} = \mathcal{B} \backslash \{s\}$
  end if
end while

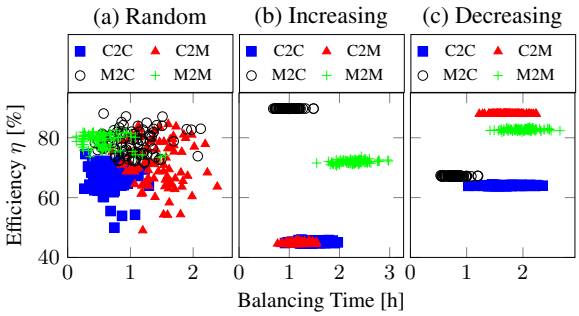


Figure 5: Profiling analysis of the different charge transfer patterns enabled by our proposed architecture.

packs having random, monotonically increasing and decreasing SoC distributions. These categories model the realistic charge variations in a battery pack typically caused by manufacturing differences and the temperature gradient due to the direction of coolant flow from either side of the pack. We used SAMSUNG INR 18650-25R cells, with a nominal capacity of 2.5 A h and a nominal voltage of 3.75 V for forming a battery pack by connecting 24 of them in parallel and 36 of these parallel-connected modules in series. The SoCs of the cells are distributed with a variance of 0.05 around an average value of 50 %. For each random, monotonically increasing and decreasing cases, 100 different SoC distribution patterns are generated, which are then equalized using the different transfer patterns enabled by our proposed architecture. The analytical model derived in Section 4 along with the equivalent resistances (R_α and R_β) shown in Fig. 3 for each type of charge transfer pattern are used to calculate the energy efficiency. Commercially available inductors (*WE-7443551131*) and MOSFETs (*NTMFS4955N*) were used in our simulation analysis whose parameters are:

$$\begin{bmatrix} \mathrm{R_B} & \mathrm{R_L} & R_\mathrm{M} & \mathrm{L} \\ I_\mathrm{peak} & \mathrm{t_{ON}} & \mathrm{t_{OFF}} & \mathrm{C_{OSS}} \end{bmatrix} = \begin{bmatrix} \frac{1}{24}22.5\mathrm{m\Omega} & 12\,\mathrm{m\Omega} & 8.5\,\mathrm{m\Omega} & 10\,\mu\mathrm{H} \\ 12\,\mathrm{A} & 35\,\mathrm{ns} & 25\,\mathrm{ns} & 483\,\mathrm{pF} \end{bmatrix}$$

Comparison of charge transfer patterns: From Fig. 5b and 5c, we can conclude that for monotonically increasing and decreasing cases, the module-to-cell and cell-to-module charge transfer patterns respectively, provide the highest possible efficiency, due to the reduced parasitic resistances along the current flow path. For instance, the module-to-cell has a reduced parasitic resistance while transferring charge from a module that is below the destination cell in the series string of the pack (Bottom-to-Top). However, for a random SoC distribution, the module-to-module transfer pattern dominates the other balancing patterns.

Algorithm 4 Hybrid charge transfer algorithm.

Input: Unbalanced SoC array $\mathcal{U}$, Maximum transfer length M, Peak balancing current, I_{peak}, Distribution pattern, $Dist$
Output: Charge transfer pairs $\mathcal{P}$

$E_\text{trans} = E_\text{loss} = 0$
if max($\mathcal{U}$)−min($\mathcal{U}$)< 0.1 % **then**
  End algorithm.
else
  switch $Dist$ **do**
    case Increasing
      $\mathcal{P}$ = Module-to-Cell transfer algorithm (Algorithm 2)
    end case
    case Decreasing
      $\mathcal{P}$ = Cell-to-Module transfer algorithm (Algorithm 1)
    end case
    case Random
      $\mathcal{P}$ = Module-to-Module transfer algorithm (Algorithm 3)
    end case
  end switch
  for $p \in \mathcal{P}$ **do**
    Calculate Q_tx (Eq. (4)) and Q_rx (Eq. (7))
    Calculate E_tx and E_diss (Eq. (11))
    $E_\text{trans} = E_\text{trans} + E_\text{tx}$
    $E_\text{loss} = E_\text{loss} + E_\text{diss}$
    Adjust $\mathcal{U}$ according to Q_tx and Q_rx
  end for
end if

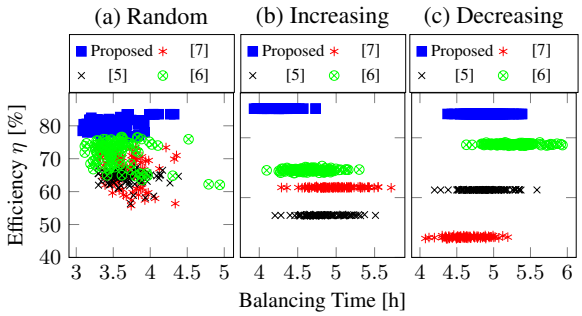


Figure 6: Comparison of our proposed balancing architecture and the hybrid equalization algorithm with state-of-the-art solutions.

5.2 Hybrid Charge Transfer Algorithm

With these observations, we propose, a system-level hybrid charge transfer algorithm in Algorithm 4 that uses the individual charge transfer strategies and automatically selects the efficient transfer pattern based on the SoC distribution. The input is the unbalanced pack and the BMS executes the charge balancing algorithm online till the difference between the SoC of cells is below a threshold value of $0.1\,\%$ (line 2). The BMS in the pack calculates the SoC of all cells to determine the type of distribution ($Dist$) and selects the appropriate strategy (line 5). Each execution of the algorithm scans the entire battery pack and fills the pair list ($\mathcal{P}$) with the selected strategy. For each pair in the pair list (line 16), the transferred charge (Q_{tx}) and the received charge (Q_{rx}) are calculated based on the Eqns. (4) and (7), respectively (line 17). With this, the energy that is transferred (E_{tx}) and the energy (E_{diss}) that is dissipated are calculated in line 18 using the Eq. (11). The overall energy transferred (E_{trans}) and the energy dissipation (E_{loss}) for all pairs are updated accordingly in lines 19 and 20. Subsequently, the SoC of the cells involved in the charge transfer process are updated (line 21) and the algorithm continues to equalize till the difference in SoC of all cells is within the allowable threshold value.

6 Case Study

In this section, we compare the efficiency of our proposed balancing architecture and the hybrid charge transfer strategy with the state-of-the-art solutions proposed in [6], [7] and [5]. In order to simulate the existing architectures using the analytical model derived in Section 4, the equivalent resistances R_α and R_β along the current flow path have to be updated with resistances of the particular architecture for different types of charge transfer patterns. For [6] and [5], the equivalent resistances when transferring charge from different source and destination cells are provided and we use them in our simulation framework. In case of the architecture in [7], we have calculated the equivalent resistance by analyzing the balancing current flow directions for different source and destination cells. We use a realistic EV battery pack of $21.6\,\mathrm{kW\,h}$ capacity for our case study and this is obtained by connecting 96 modules in series where each module is made of 24 parallel-connected SAMSUNG INR 18650-25R cells. For our case study involving cell-to-module, module-to-cell and module-to-module simulations, we considered a module to be consisting of 8 series-connected cells. The component specifications for the balancing architecture and the SoC distribution patterns are same as in the profiling analysis in Section 5.1. Please note that the architectures proposed in [7] and [5] are only capable of performing cell-to-cell charge transfers and the architecture in [6] is capable of performing all types of charge transfers except direct charge transfers between non-adjacent cells. Therefore, the cell-to-cell transfer algorithm is used for simulating the architectures in [7] and [5] and the module-to-module charge transfer strategy in Algorithm 3 is used for the many-to-many architecture in [6].

Fig. 6 shows the result of our simulation case study. Our proposed balancing architecture and the hybrid charge transfer algorithm provide significantly higher energy efficiency compared to the state-of-the-art solutions for all random, monotonically increasing and decreasing SoC distributions as shown in Fig. 6a, 6b and 6c, respectively. This is mainly due to the fact that our proposed balancing circuit is capable of performing multiple charge transfer patterns with a reduced resistance along the current flow path compared to the existing solutions. In addition, our smart equalization strategy selects the energy-efficient charge transfer pairs depending upon the SoC distribution and the characteristics of the circuit architecture, thereby further improving the energy efficiency. Table 1 shows the minimum, maximum and average energy efficiency of the balancing architectures for random, monotonically increasing and decreasing SoC distributions analyzed in this case study. From Table 1, we can observe that our proposed multi-pattern active cell balancing architecture and the hybrid equalization strategy provide an improvement in energy efficiency from $10.65\,\%$ up to a maximum of $46.83\,\%$.

Architecture	η_{eff} [%] Random			η_{eff} [%] Increasing			η_{eff} [%] Decreasing		
	Min	Max	Mean	Min	Max	Mean	Min	Max	Mean
Proposed	76.75	83.52	80.37	89.65	89.79	89.74	87.88	87.97	87.94
[7]	55.73	73.62	66.51	63.16	63.76	63.40	46.20	47.46	46.75
[5]	56.33	67.49	64.37	53.79	54.44	54.07	62.44	62.77	62.57
[6]	62.06	76.60	71.81	68.22	70.55	69.19	77.31	78.46	77.79
Average improvement [%] over existing solutions									
[7]		17.25			29.35			46.83	
[5]		19.89			39.74			28.85	
[6]		10.65			22.89			11.54	

Table 1: Our proposed architecture dominates the existing approaches for all different types of SoC distributions.

7 Concluding Remarks

In this paper, we proposed a modular, multi-pattern active cell balancing architecture that is capable of performing multiple charge transfer patterns with a reduced number of hardware components and control signals. We derived an analytical model of our proposed architecture and profiled the energy efficiencies of different charge transfer patterns towards realistic SoC distributions in a battery pack. Using this profiling analysis, we proposed a hybrid charge transfer algorithm that automatically selects the energy-efficient transfer pattern depending upon the SoC distribution of the pack. Finally, a detailed case study showed that our proposed balancing architecture and the hybrid charge transfer strategy significantly outperform existing approaches in terms of energy efficiency and balancing time for all types of realistic SoC distributions.

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