Improving Fast Charging Efficiency of Reconfigurable Battery Packs

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***Abstract*—Recently, reconfigurable battery packs that can dynamically modify the electrical connection topology of their individual cells are gaining importance. While several circuit architectures and management algorithms are proposed in the literature, the electrical characteristics of the reconfiguration circuit architectures are not sufficiently studied so far. In this paper, we derive a detailed analytical model for a state-of-the-art reconfiguration architecture capturing the losses introduced by the parasitic resistances of the circuit components. Based on this model we evaluate a novel fast charging strategy, which for the first time utilizes the reconfigurable battery pack architecture in order to reduce the losses during fast charging by switching between parallel and series connection of the cells. In order to do this, we consider the electrical characteristics of the reconfigurable circuit components. Since the component resistances are the main driver for the power losses during charging, we are able to give a realistic perspective on the overall pack performance and the efficiency increase due to the utilized fast charging strategy. Furthermore, using the analytical model, we highlight the challenges faced by existing reconfiguration architectures using state-of-the-art components and we derive specifications for the switches for further improving the energy efficiency. Experimental results show that our strategy improves the charging efficiency by up to 10 %.**

I. Introduction and related work

Electric Vehicles (EVs) are playing a central role in paving the way for a future of sustainable mobility and reduced CO_2 emissions. However, currently a widespread acceptance of EVs is obstructed by range anxiety and charging time. Therefore, the key enabling technology for EVs is fast chargeable electrical energy storage systems which dominantly come in the form of Li-Ion battery packs. While the issue of limited range is diminishing due to falling Li-Ion battery prices and consequently larger battery packs, the charging time still constitutes a grave drawback. To resolve this problem, the industry trend is moving towards fast charging technologies which allow to fully charge the battery pack in less than 20 minutes.

However, to achieve these short charging times, immense currents are required which then again result in drastically increased power losses. Fully DC-charging a 85 kWh battery (e.g. Tesla Model S) in a desired charging time of 20 minutes leads to a current of $I_\mathrm{C} \approx 700\,\mathrm{A}$. Assuming a battery pack with 96 cells in series results in power losses in the magnitude of multiple kilowatts. Since the majority of the energy dissipation originates from ohmic power losses, which are a quadratic function of the charging current, reducing this current is crucial to increase the efficiency. The difficulty hereby lies in simultaneously maintaining the short charging time.

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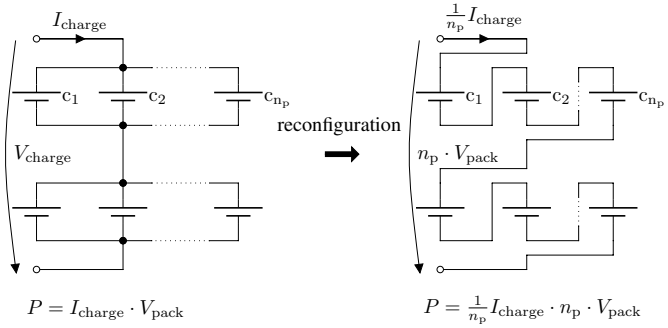

Fig. 1: Left: Battery cells in normal configuration. n_p cells in parallel and n_s cells in series.
Right: Battery cells reconfigured to turn all parallel cells to be in series ($n_\mathrm{p} \cdot n_\mathrm{s}$ cells in series). The charging current I_charge of the reconfigured circuit is by a factor n lower compared to the not reconfigured circuit.

The two conditions of reducing the current and maintaining a short charging time mean that the battery pack voltage needs to be increased. This necessity arises from the equation for electric energy $E = I \cdot V \cdot t$.

Since conventional battery packs have a static topology and thus voltage, in this paper, we utilize the three switch state-of-the-art reconfigurable battery pack architecture which was described in [1], [2]. This architecture allows to change the topology of the battery pack by switching parallel cells into serial connection, which increases the pack's voltage. This particular feature is achieved by introducing switches around each battery cell. Until now, these architectures are solely used for cell balancing purposes and as a safety measure to isolate faulty cells from the pack [3]–[7]. The application of reconfigurable battery pack architectures in fast charging scenarios to reduce power losses has not yet been sufficiently examined in literature so far.

Therefore, for the first time, in this paper we propose a novel fast charging strategy where the reconfigurable architecture is used to switch all parallel connected cells into a series connection (as shown in Figure 1) to drastically reduce the

charging current, and hence the energy dissipation, while maintaining the same charging power and time. On the one hand adding switches to the reconfigurable cell circuit, whose electric characteristics are described in detail in Section II, indeed introduces additional resistances, and thus losses. On the other hand, however, we gain the ability to utilize the advantages of the reconfigurable architecture, such as increased robustness and fault tolerance [1]. Based on this, in Section III, the fast charging strategy is described, which employs the aforementioned advantages, and in Section IV a detailed analytical model of the reconfigurable architecture is provided. With this model, we are capable to calculate the power losses based on the parasitic resistances of the circuit components. Furthermore, we are able to derive optimized specifications for the switches in the reconfigurable architecture circuit in Section V in order to improve the overall efficiency.

II. Architecture

In this section the utilized modular reconfigurable cell architecture is described. These reconfigurable cells can be interconnected similar to conventional cells and have the ability to obtain either a parallel connection or a series connection. Each reconfigurable cell consists of the battery cell and three transistors connected according to the circuit displayed in Figure 2. The cell itself is represented as a serial connection of a constant voltage source V_{OC} and an inner resistance R_{i}. Since no aging effects are taken into account this simple linear cell model is sufficient [8]. Each reconfigurable cell can operate in three different modes. For the first mode, switches S1 and S2 are closed and S3 left open. In this mode, the cells are connected in parallel. In the second mode switch S3 is closed and switches S1 and S2 are left open. Note that it is to consider that for the leftmost cell, switch S1 must be closed and for the rightmost cell, switch S2 instead of S3 must be closed, in order to complete the circuit. In this mode, all cells are connected in series. For the last mode, all switches are left open. This separates the cell from the rest of the battery pack. It is to be noted that this reconfigurable architecture is comparable to a static architecture in so far as that, in its base configuration, it also has a fixed amount of cells in series and in parallel. The special feature is that this architectures configuration can be changed to connect all cells in series.

III. Fast Charging Strategy

The novel approach to fast charging, proposed in this paper, utilizes the reconfigurable architecture introduced in Section II. The overall idea is to reduce the charging current to lower the ohmic losses.

$$P_{\mathrm{loss}} = f(I^2) \tag{1}$$

Since the ohmic losses are, according to Equation 1, quadratically proportional to the current, reducing the current yields enormous loss saving potential. Therefore we use the reconfigurable architecture to switch all parallel connected cells into a serial connection during charging. This reduces the current by the factor n_{p}, which represents the number of cells in parallel in the discharging configuration. This reconfiguration leads to a voltage increase by the same factor n_{p}, which again, multiplied with the reduced current, results in the same power which is necessary to maintain the short charging time. However, during discharging, the battery pack needs to be switched back into the initial configuration to be able to provide the necessary current and voltage in order to achieve the operating voltage of the inverter and electrical machine. This, on the other hand, has a negative impact on the efficiency of the battery pack compared to a non-reconfigurable architecture due to the ohmic losses which are introduced by the on-resistance of the transistors. Since the increased energy dissipation can be compensated by the reduced charging current, our goal is to use the already beneficial reconfigurable architecture to full capacity. In the following section, we will derive an analytical model to investigate the efficiency in detail.

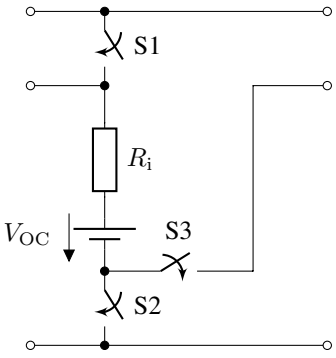

Fig. 2: Equivalent circuit of one reconfigurable battery cell. The cell operates in parallel mode when S1 and S2 are closed. Closing only switch S3 reconfigures the cell to operate in serial mode. Leaving all switches open isolates the cell from the rest of the pack.

IV. Simulation Model

Based on the circuit in Figure 2, a simulation model was implemented to calculate the ohmic losses that occur in a battery pack during charging and discharging. Therefore, a battery pack class was implemented that contains the essential parameters of each cell. Namely, these parameters are the cell open circuit voltage V_{OC}, the inner resistance R_{i}, the switches' on resistance R_{S}, the plug resistance R_{plug}, the number of cells in series n_{s} and parallel n_{p}, the number of transistors in parallel per switch S_{p}, and the capacity of the pack C_{pack}. As input parameter, the charging rate c is used, which is set to $3\,c$ as default, in order to achieve a State of Charge (SoC) of $100\,\%$ within 20 minutes. The charging rate determines the charging and discharging current I_{c} and the resulting pack voltage V_{bp}. Based on whether the pack is reconfigurable and its reconfiguration state, the equivalent resistance R_{eq} of the entire pack needs to be calculated differently. For a static pack, the equivalent resistance depends on the number of cells in series and parallel and the inner resistance of the cells. During charging, the resistance of the connecting plug is added:

$$R_{\mathrm{eq}}(n_{\mathrm{s}}, n_{\mathrm{p}}) = \begin{cases} \frac{n_{\mathrm{s}}}{n_{\mathrm{p}}} \cdot R_{\mathrm{i}}, & \text{when discharging} \\ \frac{n_{\mathrm{s}}}{n_{\mathrm{p}}} \cdot R_{\mathrm{i}} + 2 \cdot R_{\mathrm{plug}}, & \text{when charging} \end{cases} \tag{2}$$

This value for the equivalent resistance leads to the calculation of the overall pack voltage as follows:

$$V_{\mathrm{bp}} = V_{\mathrm{OC}} \cdot n_{\mathrm{s}} + R_{\mathrm{eq}} \cdot I_{\mathrm{c}} \tag{3}$$

For a reconfigurable pack with a cell circuit shown in Figure 2, the equivalent resistance depends on whether the pack is reconfigured (charging) or not (driving). During driving, the battery pack is in its initial configuration with multiple cells in parallel. The equivalent resistance can then be calculated as follows:

$$R_{\mathrm{eq}}(n_{\mathrm{s}}, n_{\mathrm{p}}) = (R_{\mathrm{i}} + R_{\mathrm{S1}} + R_{\mathrm{S2}}) \cdot \frac{n_{\mathrm{s}}}{n_{\mathrm{p}}} \tag{4}$$

In order to calculate the overall battery pack voltage for this configuration, Equation 3 can be used again. During charging on the other hand, the battery pack gets reconfigured and all cells are connected in series. The resulting equivalent resistance in that case can be determined with the help of

$$R_{\mathrm{eq}}(n_{\mathrm{s}}, n_{\mathrm{p}}) = n_{\mathrm{cells}} \cdot R_{\mathrm{i}} + n_{\mathrm{s}} \cdot (R_{\mathrm{S1}} + R_{\mathrm{S2}}) + n_{\mathrm{s}} \cdot (n_{\mathrm{p}} - 1) \cdot R_{\mathrm{S3}} \tag{5}$$

where $n_{\mathrm{cells}} = n_{\mathrm{s}} \cdot n_{\mathrm{p}}$ is the total number of cells. For this case also the overall pack voltage needs to be calculated differently. This can be achieved with the following equation:

$$V_{\mathrm{bp}} = V_{\mathrm{OC}} \cdot n_{\mathrm{cells}} + R_{\mathrm{eq}} \cdot I_{\mathrm{c}} \tag{6}$$

After obtaining the battery pack voltages, both for reconfigurable and static packs, the voltage drop over the connection plug during charging can be added. This leads to the charging voltage V_{c}, with

$$V_{\mathrm{c}} = V_{\mathrm{bp}} + 2 \cdot R_{\mathrm{plug}} \cdot I_{\mathrm{c}}. \tag{7}$$

Consequently the overall pack charging power P_{c} is the result of the product of charging voltage and charging current: $P_{\mathrm{c}} = V_{\mathrm{c}} \cdot I_{\mathrm{c}}$.

The next step is to determine the power losses that occur during charging. In this model we focus on the ohmic power losses which originate from the transistor on-resistance and the connector plug resistance. Since we want to investigate the impact different parameters have on the power losses, the model is able to iterate through various parameters and display the result. The power loss calculation is implemented analogous to the aforementioned battery pack voltage calculation and follows the equation for ohmic losses in a resistor $P = I^2 \cdot R$. With Equation 2 this leads, for the case of charging a static battery pack, to power losses $P_{\mathrm{l,c}}$ as follows:

$$P_{\mathrm{l,c}} = \frac{C_{\mathrm{pack}} \cdot c \cdot {n_{\mathrm{P}}}^2}{n_{\mathrm{cells}} \cdot V_{\mathrm{OC}}} \cdot \left(\frac{n_{\mathrm{S}}}{n_{\mathrm{P}}} \cdot R_{\mathrm{i}} + 2 \cdot R_{\mathrm{plug}}\right) \tag{8}$$

Similarly, the power losses $P_{\mathrm{l,reconfig,c}}$ that occur during charging the reconfigurable pack can be calculated with:

$$P_{\mathrm{l,reconfig,c}} = \frac{C_{\mathrm{pack}} \cdot c}{c_{\mathrm{cells}} \cdot V_{\mathrm{OC}}}^2 \cdot (n_{\mathrm{cells}} \cdot R_{\mathrm{i}} + n_{\mathrm{s}} \cdot (R_{\mathrm{S1}} + R_{\mathrm{S2}}) + n_{\mathrm{s}} \cdot (n_{\mathrm{P}} - 1) \cdot R_{\mathrm{S3}} + 2 \cdot R_{\mathrm{plug}}) \tag{9}$$

Besides the ability to calculate the losses occurring during charging, the model is also able to calculate the discharging losses for a variety of different EV use cases over a driving cycle. The EVs in particular are Nissan Leaf, Kia Soul, Tesla Model S and a fully electric Bus. The driving cycles are taken from the Worldwide harmonized Light vehicles Test Procedure (WLTP), and it can be chosen between Class 1, for low and medium speeds, Class 2, for low to high speeds and Class 3, for the most diverse test cycle with very high speeds. For the electric bus, a synthesized driving cycle is used, which represents the acceleration and deceleration behavior between two stops.

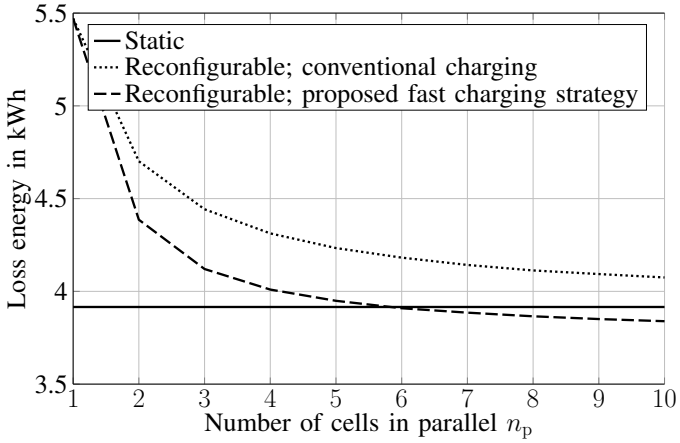

Fig. 3: Energy losses depicted over different initial pack configurations with n_{p} cells in parallel. The continuous line shows the loss energy for a static battery pack without switches. The dotted and dashed lines represent the loss energy behavior of the reconfigurable architecture with and without our fast charging strategy.

V. Results

We have implemented the model, described in Section IV, entirely in python and achieved a runtime for one charge-discharge cycle of less than one second. Figure 3 shows the results of the energy loss calculation over one full charge cycle for a conventional static battery pack, a reconfigurable battery pack without using the proposed fast charging strategy and a battery pack using the fast charging strategy. The loss energy is calculated for different base configurations of the battery pack with a varying number of cells in parallel n_{p}. For all packs, a capacity of 85 kWh is assumed. The figure shows that applying the fast charging strategy and switching all n_{p} cells in series yields a significant loss reduction potential over existing utilization of the reconfigurable architecture. The loss reduction can reach up to 10 %. Figure 3 furthermore shows that for a certain value for n_{p}, the fast charging strategy even results in lower losses than a conventional static battery pack. In this particular case any value $n_{\mathrm{p}} > 6$ is beneficial for the performance.

In order to analytically compare the charging efficiency of our fast charging strategy using the reconfigurable architecture to the efficiency of a static battery pack, we can look at what point the graphs from the power losses in Equation 8 and 9 intersect. Furthermore we can investigate which condition needs to be fulfilled in order for the reconfigurable architecture

to be more efficient during charging. Therefore we set the quotient of both power losses to be greater than one:

$$\frac{P_{\mathrm{l,c}}}{P_{\mathrm{l,reconfig,c}}} \overset{!}{>} 1 \tag{10}$$

Inserting Equations 8 and 9 into this inequation and subsequently eliminating the term for the charging current, results in:

$$\frac{n_{\mathrm{P}}^2(\frac{n_{\mathrm{S}}}{n_{\mathrm{p}}}R_{\mathrm{i}} + 2R_{\mathrm{plug}})}{n_{\mathrm{cells}}R_{\mathrm{i}} + n_{\mathrm{s}}(R_{\mathrm{S1}} + R_{\mathrm{S2}}) + n_{\mathrm{s}}(n_{\mathrm{p}} - 1)R_{\mathrm{S3}} + 2R_{\mathrm{plug}}} > 1 \tag{11}$$

Assuming all switches in the reconfiguration circuit are the same and therefore have the same on-resistance R_{on}, we can simplify this inequation even further:

$$\begin{aligned} &\text{with } R_{\mathrm{S1}} = R_{\mathrm{S2}} = R_{\mathrm{S3}} = \frac{R_{\mathrm{S}}}{S_{\mathrm{P}}} = R_{\mathrm{on}} \\ &\Rightarrow R_{\mathrm{on}} < \frac{2R_{\mathrm{plug}}(n_{\mathrm{p}} - 1)}{n_{\mathrm{s}}} \end{aligned} \tag{12}$$

This equation illustrates the fundamental relation between on-resistance, plug resistance and the initial topology of the battery pack and shows the options on how to improve the efficiency of the reconfigurable battery pack even further. Either increasing the number of cells in parallel n_{p} or decreasing the number of cells in series n_{s} are viable options to improve the efficiency. The other option is to optimize the switches regarding their on-resistance. Both options yield potential to improve the energy efficiency of the reconfigurable battery architecture using the proposed fast charging strategy even further.

Calculating the losses for an entire charge and discharge cycle for different EVs and plotting the loss reduction between a static pack and the reconfigurable architecture with fast charging strategy results in the graphs in Figure 4. Since the resistances of the switches, the plug and number of cells in series are constant for this calculation, and only the mechanical model of the vehicle differs, the point where the graphs intersect the baseline is almost constant, which confirms the findings of Equation 12. On the left side of this point, where $n_{\mathrm{p}} < 6$, the static battery pack outperforms the reconfigurable architecture, whereas beyond that point ($n_{\mathrm{p}} > 6$) the reconfigurable architecture has an advantage over the static battery pack. The total loss reduction is indeed very minor especially for EVs with smaller capacity battery packs. The figure, however, shows that with increasing pack capacity the potential loss reduction also increases drastically, which makes the reconfigurable architecture especially interesting for electric public transport applications.

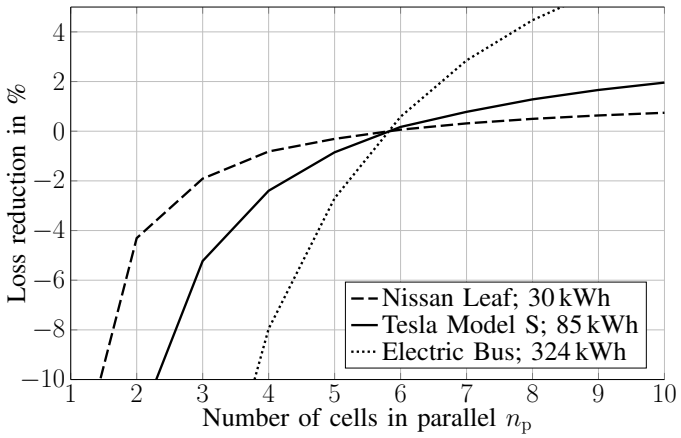

Fig. 4: Reduction of the losses over one charge-discharge cycle compared between the reconfigurable architecture with fast charging strategy and a static battery pack for different EV use cases.

VI. Conclusion

In this paper we have introduced a novel fast charging strategy for reconfigurable battery pack architectures, which for the first time utilized the reconfigurability to switch parallel connected cells into a series connection, in order to reduce the current during charging. This fast charging strategy allowed us to add an overall efficiency gain of around 10 %, in addition to the already present advantages, compared to existing reconfigurable architectures. Under certain circumstances, we are able to even be on a par with conventional static battery pack architectures regarding power losses. We have specified an exact expression for the on-resistance of the switches in the reconfigurable circuit, which gives us the ability to determine concrete resistance values to evaluate the energy efficiency of the reconfigurable battery architecture. Future development in transistor technology, especially regarding their resistance, would augment the advantages of the reconfigurable architecture even further.

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